REMARKS

Reconsideration and allowance of the subject application are respectfully requested. Upon entry of this Amendment, claims 1-13 are pending in the application. In response to the Office Action (Paper No. 6), Applicant respectfully submits that the pending claims define patentable subject matter. By this Amendment, Applicant has amended claims 1, 2, 6 and 11 to improve clarity.

I. Preliminary Matters

Attached to the Office Action was a signed copy of the PTO-1449 Form submitted with the Information Disclosure Statement filed on September 23, 1999. However, that the Examiner did not initial the four references listed in the "Other Documents" section on the PTO-1449 Form. Accordingly, Applicant requests that the Examiner initial these reference and send a corrected copy of the PTO-1449 Form along with the next Action.

II. The Present Invention

The present invention is directed to a method and device for generating ATM cells for low bit rate connections having different priorities. In particular, two streams of CPS packets are multiplexed into a same ATM connection, wherein one stream of CPS packets CPS_0 corresponds to real time, or high priority, traffic (for example speech traffic) and the other stream of CPS packets CPS_1 corresponds to non real time, or low priority, traffic (such as for example data traffic or signaling). In the following, index 0 will be used for high priority traffic, and index 1 will be used for low priority traffic.

As shown in Figure 1, when CPS packets from the streams CPS_0 or CPS_1 arrive, they are stored in a common buffer CB and a pointer 2_0 or 2_1 to the CPS packet or address @ of the CPS packet in the common buffer CB is inserted in a corresponding FIFO memory, or linked list, LL_0 or LL. The linked list LL_o contains all the addresses of high priority CPS packets competing for packing into ATM cells and the linked list LL_1 contains all the addresses of low priority CPS packets competing for packing into ATM cells. A computation means 3 determines new value of sum of length indicators SLI_0 and SLI_1 indicating a sum of the lengths of all CPS packets of linked lists LL_0 and LL_1 by adding length Lli of the received CPS packet.

At each scheduled cell transmission time AST, linked lists LL_0 and LL_1 are served according to their respective priority and an ATM cell is filled accordingly. In other words, every ATM cell scheduled transmission time, multiplexing means 8 maps the selected octets into ATM cells according to the following rules.

If $SLI_o \geq 47$ octets (i.e., if $SLI_o \geq$ number of octets of an ATM cell payload), the addresses in the common buffer of the first received 47 octets of high priority are read in linked list LL_0, the common buffer CB is "emptied" from these 47 first octets, SLI_0 is set to SLI_0- 47, and these octets are mapped into an ATM cell without padding.

If $SLI_o < 47$ octets (with $SLI_0 = x$), the addresses in the common buffer of the "x" first received octets of high priority are read in linked list LL_0, the common buffer CB is "emptied" from these "x" octets, and SLI_0 is set to zero. Further, if $SLI_1 = 0$, i.e. if there are no low priority packets to fill the cell, these "x" octets are mapped into the ATM cell and padding is used in this case to fill the cell. If $SLI_1 > 0$ and $SLI_1 \geq 47$-x, the addresses in the

common buffer of the first 47-x received octets of low priority are read in linked list LL_1, the common buffer CB is "emptied" from these octets, SLI_1 is set to SLI_1 =SLI1-(47-x), and these "x" and 47-x octets are mapped into the ATM cell without padding. If $SLI_1 > 0$ and $SLI_1 <$ 47-x (with $SLI_1 = y$), the common buffer is emptied from the corresponding "y" octets, SLI_1 is set to 0, and these "x" and "y" octets are mapped into the ATM cell and padding is used to fill the rest of the cell.

In another embodiment shown in Figure 2, intra priority multiplexing is carried out at ATM Adaptation Layer (AAL) level, and the inter-priority multiplexing is carried out at ATM Layer level. The method illustrated in Figure 2 differs from the one illustrated in Figure 1 in that two types of ATM cells are created by intra-priority multiplexing (i.e. by multiplexing of CPS packets of the same priority) each type corresponding to a type of traffic priority, and these two types of ATM cells are multiplexed into an ATM connection at ATM layer level. A first type of ATM cells ATM_{n0} corresponds to high priority traffic, and a second type of ATM cells ATM_{n1} corresponds to low priority traffic. The ATM cells ATM_{n0} and ATM_{n1} are formed using queuing means 5_0 and 5_1 and multiplexing means 9_0 and 9_1 that do not apply any traffic priority criteria, respectively. The ATM cells ATM_{n0} and ATM_{n1} are multiplexed at the ATM layer level uses queuing means 6_0 and 6_1 by multiplexing means 7 that do apply traffic priority criteria.

III. Prior Art Rejections

A. Disclosure of Petersen

Petersen is directed to a method and apparatus for segmenting, multiplexing and transporting user data packets in an ATM telecommunication system by assigning a transmission priority code to each segmented user data packet based on the type of data contained therein. Data that is highly sensitive to transmission delays (e.g., voice data) will be assigned a high priority, while data that is less sensitive to transmission delays (e.g., signal strength measurement data) will be assigned a lower priority. When the user data packet segments are assembled into segment minicells and multiplexed into the ATM cell stream, those with the highest priority will be inserted first so that they experience the least amount of transmission delay.

As shown in Figure 6, a minicell transmission sequence 600 is formed by segmenting, assembling, and multiplexing user data packet "a" 605 and user data packet "b" 610, wherein user data packet "a" 605 arrives at an ATM adaptation layer (AALm) before user data packet "b" 610. A segmentation and reassembly (SAR) sublayer immediately begins to divide user data packet "a" 305 into three segments upon arrival. An assembly and disassembly (AAD) sublayer then begins assembling the three segments into minicells 1a, 2a, and 3a respectively, and a multiplexing and demultiplexing (MAD) sublayer 203 begins multiplexing the minicells 1a, 2a, and 3a into the ATM cell stream for transmission. However, before minicell 2a has been fully segmented, assembled, and multiplexed, user data packet "b" 610 arrives at the AALm, wherein user data packet "b" 610 has a higher transmission priority than user data packet "a" 605. The AALm recognizes that user data packet "b" 610 has a higher priority and immediately interrupts

the processing of user data packet "a" 605 until user data packet "b" has been segmented, if necessary, assembled into a minicell b, and multiplexed into the ATM stream for transmission. Once this has been accomplished, the AALm will complete the processing of user data packet "a" 605, assuming that no additional user data packets with a higher priority have arrived. Thus, minicell b is multiplexed into the ATM cell stream ahead of minicell 2a and minicell 3a so that the voice data contained in the payload of minicell b will arrive at the receiving station prior to the data of minicell 2a and minicell 3a.

The simultaneously multiplexing of more than one user data packet on a single minicell connection is performed as a function of transmission priority by employing a predefined transmission priority assignment schedule (see TABLE 1). A length code is used to define the length of each segment and the relative position of each segment (i.e., whether the segment is a first, middle, or last segment) as well as the transmission priority of the corresponding user data packet.

As shown in Figure 9 illustrating an apparatus 900 used to implement the method described above, a user data packet 905 arrives at an AALm layer 910 from an application layer 912. Attached to the user data packet 905 is a user data packet pointer 915 which contains a number of bits which define the minicell connection identifier (CID) associated with the user data packet 905. The pointer 915 also defines the type of data contained in the user data packet 905 (e.g., voice data, circuit data, power measurement data, control data, etc.), which in turn defines the transmission priority for user data packet 905, and the length of the user data packet 905.

At the AALm 910, a FIFO-IN 920 receives user data packet 905. In practice, FIFO-IN buffer 920 will receive user data packets from many applications operating simultaneously. Once stored in the FIFO-IN buffer 920, the pointer is removed and analyzed by a control logic 922. A sort multiplexer 925 then begins dividing the user data packet 905 into segments whose lengths are determined by the control logic 922. A sort multiplexer 925 also pads the last segment of user data packet 905 and as directed by the control logic 922. The segments are then assembled into minicells and the appropriate minicell headers are attached thereto. The sort multiplexer 925 then transfers the assembled minicells to one of a plurality of FIFO-OUT buffers 930 corresponding to each transmission priority category as instructed by control logic 922 which determines the appropriate the FIFO-OUT buffer 930 based on the priority of the user data packet 905.

A priority multiplexer 935 then selects minicells according to priority, wherein if a higher priority FIFO-OUT buffer 930 contains minicells, the priority multiplexer 935 will select these minicells and multiplex them into the payload of the current ATM cell 940. If the higher priority FIFO-OUT buffer 930 is empty, the priority multiplexer 935 will move to the next highest FIFO-OUT buffer 930 for selecting minicells. An ATM layer 945 attaches an ATM header to each ATM cell payload before transmitting the ATM cell 940 to a receiving station.

B. Disclosure of Depelteau et al.

Depelteau et al. (USP ,6404,767; hereafter "Depelteau") discloses a system and method for implementing available bit rate (ABR) flow control in ATM switches. A partitioned architecture

a featuring standalone ABR processing subsystem allows components to be changed with little impact on the switch's overall design. Both end-to-end and virtual source/virtual destination (VS/VD) flow control systems are provided as are both configurations for switches which are either standalone or connected to a switching fabric.

As shown in Figure 1, the ATM network includes a source 10, a network 11 having a number of switches 12,14,16, and a destination 18. When the source 10 initially decides it needs to communicate with the destination 18, a forward virtual connection is established from the source to the destination and a reverse virtual connection is established from the destination to the source. During the setup of the forward virtual connection 20, the source 10 may request an initial cell rate (ICR) and a number of RM (NRM) cells which determines the frequency with which RM cells are generated. There may be some negotiation between the source 10, the switches 12, 14 and destination 18 before agreed upon values for ICR and NRM are established.

The source 10 may then begin sending cells at the negotiated ICR. Every NRM cells, the source 10 generates an RM cell and transmits the cell towards the destination over the forward connection 20. While the RM cell is travelling to the destination 18 it is referred to as a forward RM (FRM) cell. At the destination 18, the RM cell is turned around and travels from the destination back to the source 10 along the reverse connection 22, and during this time it is referred to as a backwards RM (BRM) cell. The forward connection 20 carries the source's traffic cells, the source's FRM cells, and the destination's BRM cells. The reverse connection 22 carries the source's BRM cells, and the destination's traffic cells and the destination's FRM cells.

When the source 10 receives the BRM cell, it reads an explicit rate (ER) in the BRM cell and adjusts its allowed cell rate (ACR) accordingly. The ACR is the maximum rate at which the source may send cells and is initially set to equal the ICR. It will then adjust its current cell rate (CCR) if necessary to ensure that it is less than or equal to the ACR. The CCR is the rate at which the source is actually transmitting cells. If the new ACR is below the CCR then the CCR must be decreased. If the new ACR is above the previous CCR, then the CCR may be increased. RM cells are generated on a per ABR connection basis. An ATM switch may have a plurality of input ports and a plurality of output ports. Each input port receives ingress cells, possibly including ABR traffic and RM cells from a number of connections. The switch routes the ingress cells from all of the input ports to the appropriate output ports where they exit the switch as egress cells. It is important that the traffic being routed to a particular output port does not exceed that output port's capacity for extended periods of time.

Each port has a fixed output capacity. At any instant in time, portions of this capacity must be allocated to various traffic classes including for example VBR, CBR and ABR. Each virtual connection of any type including ABR is always guaranteed its MCR. For each port, high priority traffic such as VBR and CBR is serviced first. The MCR for ABR connections may be also considered part of the high priority traffic to be serviced by the port. Any traffic on an ABR connection above and beyond the connection's MCR is lower priority traffic, or "ABR elastic traffic".

C. Disclosure of Harth et al.

Harth et al. (USP 6,331,981; hereafter "Harth") is directed to a method and network component for switching low bit rate connections between input modules and output modules in a communication network. The input modules and the output modules form a first switching level, and an ATM switching stage arranged between the input modules and the output modules forms a second switching level. In the first switching level, a number of low bit rate connections at the input module, which are to be transmitted to the same output module, are respectively merged by the input module into at least one ATM connection. In the second switching level, the switching through of the ATM connections for transmitting data in ATM cells ensues by the ATM switching stage. Subsequently, in the first switching level, the ATM connections which have been switched through are converted by the output module into the low bit rate connections. The combined switching in two switching levels represents an especially economical solution for functions specific to mobile radio and switching applications dealing with low bit rate traffic, by simultaneously assuring an acceptable speech quality with good exploitation of the ATM bandwidth.

D. Analysis

Claims 1, 7 and 11 are rejected under 35 U.S.C. § 102(b) as being anticipated by Petersen et al. (USP 5,802,051; hereafter "Petersen"). Claims 2-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Petersen in view of Depelteau. Claims 12 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Petersen in view of Depelteau and Harth. Applicant

respectfully submits that the claimed invention would not have been anticipated by or rendered obvious in view of the applied references.

Independent claims 1 and 11 are directed to a method and apparatus for generating ATM cells for low bit rate applications. Claims 1 and 11 recite "scheduling ATM cell transmission times in a way as to keep ATM cell spacing as constant as possible", and "multiplexing a plurality of low bit rate connections into a same ATM connection having the thus scheduled ATM cell transmission times." Applicant respectfully submits that the applied references do not teach these features of the claimed invention.

The differences between Petersen (the primary reference in each of the rejections) and the present invention can be understood by referring, for example, to Figure 9 of Petersen. Petersen's object is the preparation of the content of ATM cells noted 940 in Figure 9, in the circumstances by multiplexing of mini-cells, taking into account the respective priorities (as illustrated for example) by the blocks located on the left-hand side of ATM cells 940 in figure 9).

Contrary to the present invention, Petersen's object is not the scheduling of transmission times of such ATM cells. As for the scheduling of transmission times of such ATM cells, as indicated in the present application (in particular pages 1 and 2), a currently used solution is the following. If an ATM cell is complete with CPS packets before the expiration of a timer delay, it is sent out immediately; otherwise it is sent out (completed with padding) as soon as this timer delay expires. In other words, this solution ensures that CPS packets wait at most the duration of the timer before being scheduled for transmission. Although this solution reduces the waiting time of CPS packets, it still has the drawback of introducing some delay variations.

The present invention is based on a different approach, enabling in particular to avoid such a drawback. That is, contrary to the above-recalled prior art solution based on the use of a timer, the present invention schedules ATM cell transmission times in a way as to keep ATM cell spacing as constant as possible. In particular, the ATM cell spacing can be kept as close as possible to a cell rate negotiated for the corresponding ATM connection. Cell rate is a currently known parameter of a traffic agreement negotiated for data transfer in ATM networks. Control of compliance with the negotiated cell rate is usually performed in transit nodes of an ATM network, by compensating for cell delay variations occurring during transit in this network. On the contrary, the present invention is carried out in a source node. Indeed, the present invention is concerned with a mode of generation of ATM cells which may, in itself, introduce cell delay variations. Ensuring compliance with the negotiated cell rate, as from the source, therefore constitutes a simple and efficient way of avoiding such delay variations, while at the same time simplifying traffic management in the network.

Petersen, alone or combined with Depelteau and Harth, does not disclose or suggest such a method or apparatus for scheduling of transmission times of such ATM cells, as claimed. Accordingly, Applicant respectfully submits that independent claims 1 and 11, as well as dependent claims 2-7, 12 and 13, should be allowable because the applied references do not teach or suggest all of the features of the claims.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

Page 7, fourth full paragraph:

The second embodiment of the present invention, illustrated in figure 2, corresponds to the case where [said] said intra priority multiplexing is carried out at ATM Adaptation Layer (AAL) level, and said inter-priority multiplexing is carried out at ATM Layer level.

IN THE CLAIMS:

The claims are amended as follows:

1. (Amended) A method for generating ATM cells for low bit rate applications, said method [- including a step of] comprising:

scheduling ATM cell transmission times in a way as to keep ATM cell spacing as constant as possible, and

[a step of] multiplexing a plurality of low bit rate connections into a same ATM connection having the thus scheduled ATM cell transmission times.

2. (Amended) A method according to claim 1, wherein said ATM cell spacing is kept as close as possible to a cell rate [negociated] negotiated for the corresponding ATM connection.

6. (Amended) A method according to claim 2, wherein said cell rate may be [re-negociated] renegotiated.

11. (Twice Amended) A device for generating ATM cells for low bit rate applications, said device [including, for performing a method according to,] comprising:

means for scheduling ATM cell transmission times in a way as to keep ATM cell spacing as constant as possible, and

means for multiplexing a plurality of low bit rate connections into a same ATM connection having the thus scheduled ATM cell transmission times.